

CLAIMS

What is claimed is:

Sub A

1 1. A memory module controller for interfacing a plurality of memory
2 device on a memory module with a system memory bus coupled to a system
3 memory module, the memory module controller comprising:
4 first interface circuitry configured to receive from the system memory
5 bus a first memory transaction having a first format; and
6 control logic coupled to the first interface circuitry and generating a
7 second memory transaction for the plurality of memory devices, wherein the
8 second memory transaction corresponds to the first memory transaction and
9 has a second format different than the first format of the first memory
10 transaction.

1 2. The memory module controller of claim 1, further comprising second
2 interface circuitry coupled to the control logic and configured to transmit the
3 second memory transaction to at least one of the plurality of memory devices.

1 3. The memory module of claim 1, wherein the first memory transaction
2 includes time multiplexed address and command information.

1 4. The memory module controller of claim 3, wherein the first interface
2 circuitry comprises request handling logic that separates the address and
3 command information and provides the separate address and command
4 information to the control logic.

1 5. The memory module controller of claim 4, wherein the first memory
2 transaction further includes time multiplexed data information, and wherein

3 the request handling logic further separate the data information and provides
4 the separate data information to the control logic.

1 6. The memory module controller of claim 1, wherein the first interface
2 circuitry comprises handshaking logic provides a handshake signal to the
3 system memory bus that indicates when the memory module controller is
4 communicating data to the system memory bus.

1 7. The memory module controller of claim 1, wherein the first interface
2 circuitry comprises data handling logic configured to receive data of the first
3 memory transaction from the system memory bus and reformat the data for
4 the second memory transaction.

1 8. The memory module controller of claim 1, further comprising a write
2 buffer coupled to the first interface circuitry and storing data sent with the
3 first memory transaction.

1 9. The memory module controller of claim 8, further comprising an
2 address storage unit coupled to the write buffer and the first interface
3 circuitry, the address storage unit storing addresses associated with the write
4 data stored in the write buffer.

1 10. The memory module controller of claim 1, further comprising a read
2 buffer coupled to the control logic, the read buffer storing data read from at
3 least one of the plurality of memory devices.

1 11. The memory module controller of claim 1, further comprising a clock
2 generator coupled to the control logic and configured to receive a first clock
3 signal from the system memory bus, the clock generator circuit generating a
4 second clock signal for the plurality of memory devices.

1 12. A memory module controller for interfacing a plurality of memory
2 device on a memory module with a system memory bus coupled to a system
3 memory module, the memory module controller comprising:

4 means for receiving from the system memory bus a first memory
5 transaction having a first format; and
6 means for generating a second memory transaction for the plurality of
7 memory devices, wherein the second memory transaction corresponds to the
8 first memory transaction and has a second format different than the first
9 format of the first memory transaction.

1 13. A memory module controller for interfacing a plurality of memory
2 devices on a memory module with a system memory bus coupled to a system
3 memory module, the memory module controller comprising:

4 first interface circuitry configured to receive from the system memory
5 bus a first memory transaction; and
6 control logic coupled to the first interface circuitry and reformatting the
7 first memory transactions for the plurality of memory devices.

1 14. The memory module controller of claim 13, further comprising second
2 interface circuitry coupled to the control logic and configured to receive from
3 one of the plurality of memory devices a second memory transaction,
4 wherein the control logic reformats the second memory transaction for the
5 system memory bus.